National Semiconductor

LP2995
DDR Termination Regulator

General Description

The LP2995 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2995 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DDR DIMMS.

Patents Pending

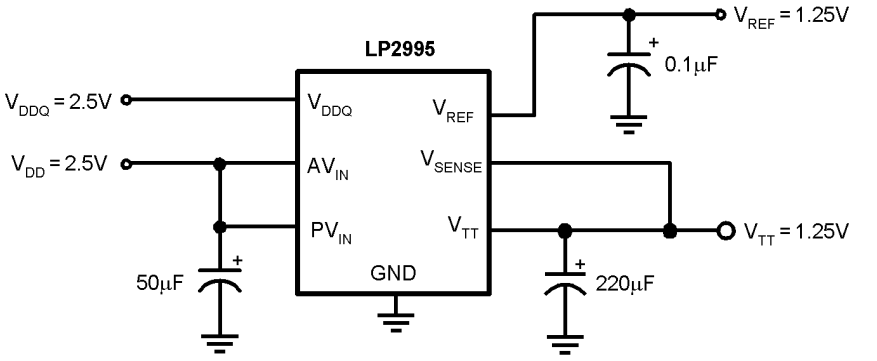
Features

- Low output voltage offset
- Works with +5v, +3.3v and 2.5v rails
- Source and sink current
- Low external component count
- No external resistors required
- Linear topology
- Available in SO-8, PSOP-8 or LLP-16 packages
- Low cost and easy to use

Applications

- DDR Termination Voltage
- SSTL-2
- SSTL-3

Typical Application Circuit



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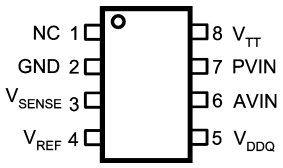
Connection Diagrams

SO-8 (M08A) Package



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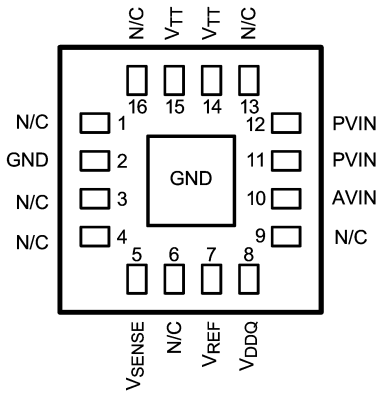
Top View

LQA- 16 Package



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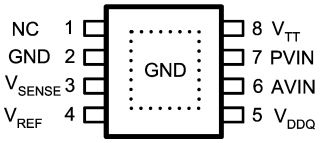
Top View

PSOP-8 (MRA08A) Package



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Top View

Pin Descriptions

SO-8 Pin or PSOP-8 Pin	LLP Pin	Name	Function
1	1,3,4,6,9, 13,16	NC	No internal connection. Can be used for vias.
2	2	GND	Ground.
3	5	VSENSE	Feedback pin for regulating VTT.
4	7	VREF	Buffered internal reference voltage of VDDQ/2.
5	8	VDDQ	Input for internal reference equal to VDDQ/2.
6	10	AVIN	Analog input pin.
7	11, 12	PVIN	Power input pin.
8	14, 15	VTT	Output voltage for connection to termination resistors.
	EP	EP	Exposed pad thermal connection. Connect to soft Ground.

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LP2995M	SO-8	M08A	95 Units per Rail
LP2995MX	SO-8	M08A	2500 Units Tape and Reel
LP2995MR	PSOP-8	MRA08A	95 Units per Rail
LP2995MRX	PSOP-8	MRA08A	2500 Units Tape and Reel
LP2995LQ	LLP-16	LQA16A	1000 Units Tape and Reel
LP2995LQX	LLP-16	LQA16A	4500 Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

PVIN, AVIN, VDDQ to GND	−0.3V to +6V
Storage Temp. Range	−65˚C to +150˚C
Junction Temperature	150˚C
PSOP-8 Thermal Resistance (θ_{JA})	43˚C/W
SO-8 Thermal Resistance (θ_{JA})	151˚C/W
LLP-16 Thermal Resistance (θ_{JA})	51˚C/W
Lead Temperature (Soldering, 10 sec)	260˚C
ESD Rating (Note 7)	1kV

Operating Range

Junction Temp. Range (Note 5)	0˚C to +125˚C
AVIN to GND	2.2V to 5.5V
PVIN to GND	2.2V to AVIN

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0˚C to +125˚C). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V (Note 6).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	I_{REF_OUT} = 0mA	**1.21**	1.235	**1.26**	V
VOS_{VTT}	V_{TT} Output Voltage Offset	I_{OUT} = 0A (Note 2)	−15 **−20**	0	15 **20**	mV
$\Delta V_{TT}/V_{TT}$	Load Regulation (Note 3)	I_{OUT} = 0 to 1.5A		0.5		%
		I_{OUT} = 0 to −1.5A		−0.5		
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = −5µA to +5µA		5		kΩ
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_q	Quiescent Current	I_{OUT} = 0A (Note 4)		250	**400**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: V_{TT} offset is the voltage measurement defined as V_{TT} subtracted from V_{REF}.

Note 3: Load regulation is tested by using a 10ms current pulse and measuring V_{TT}.

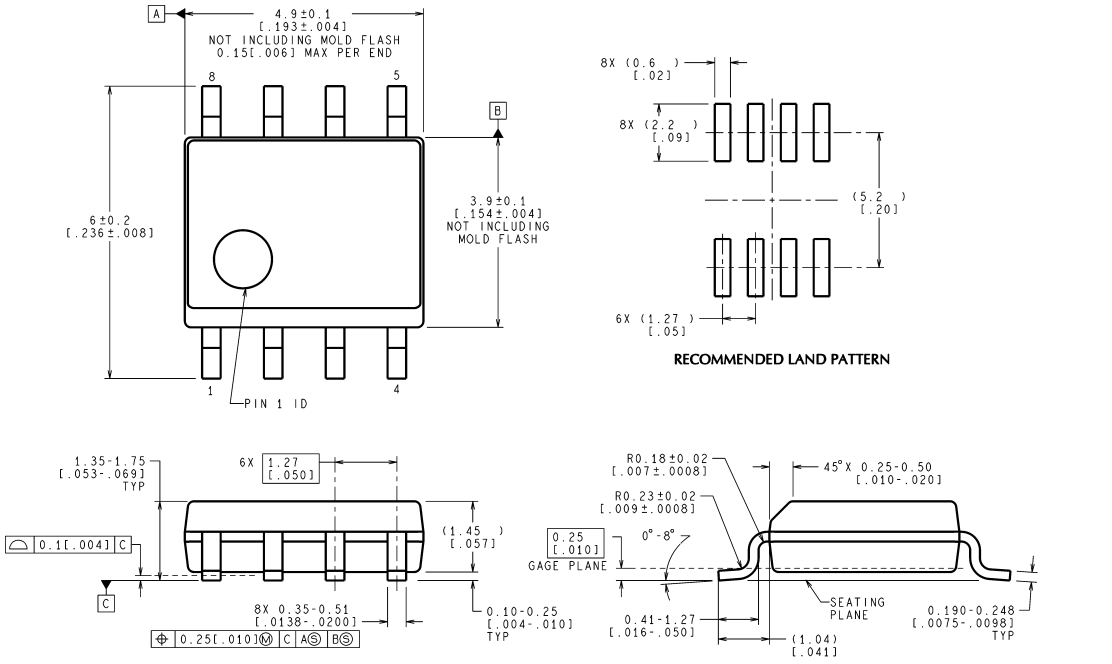
Note 4: Quiescent current defined as the current flow into AVIN.

Note 5: At elevated temperatures, devices must be derated based on thermal resistance. The device in the SO-8 package must be derated at θ_{JA} = 151˚ C/W junction to ambient with no heat sink. The device in the LLP-16 must be derated at θ_{JA} = 51˚ C/W junction to ambient.

Note 6: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 7: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

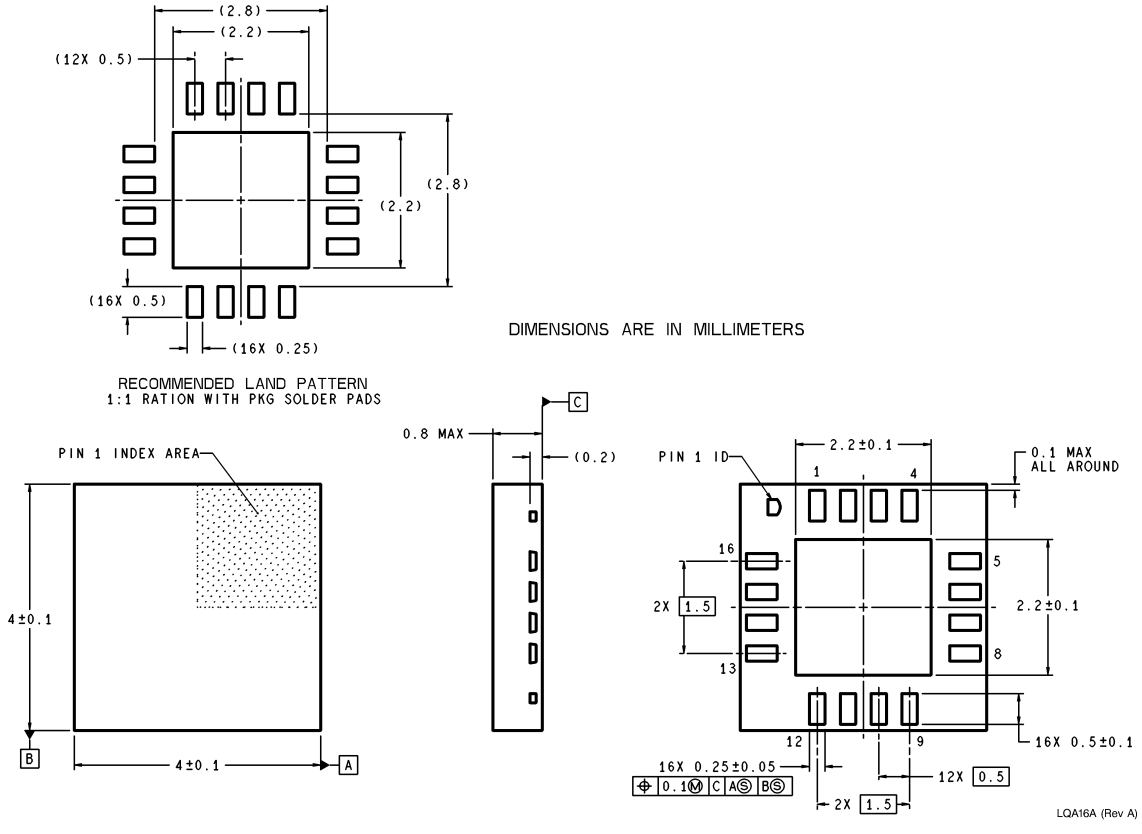
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev K)

8-Lead Small Outline Package (M8)
NS Package Number M08A



LQA16A (Rev A)

16-Lead LLP Package (LD)
NS Package Number LQA16A